

ABSTRACT

An integrated circuit and a method of manufacturing the integrated circuit, the method including: (a) providing a substrate; (b) forming a copper diffusion barrier layer on the substrate; (c) forming a dielectric layer on a top surface of the copper diffusion barrier layer; (d) forming a copper damascene or dual damascene wire in the dielectric layer, a top surface of the copper damascene or dual damascene wire coplanar with a top surface of the dielectric layer; (e) forming a first capping layer on the top surface of the wire and the top surface of the dielectric layer; (f) after step (e) performing one or more characterization procedures in relation to said integrated circuit; and (g) after step (e) forming a second capping layer on a top surface of the first capping layer.